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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : A61B 5/00 — A1

(11) International Publication Number: **WO 00/59370**

(43) International Publication Date: 12 October 2000 (12.10.00)

(21) International Application Number: PCT/GB00/01268

(22) International Filing Date: 5 April 2000 (05.04.00)

(30) Priority Data:
9907815.6 6 April 1999 (06.04.99) GB

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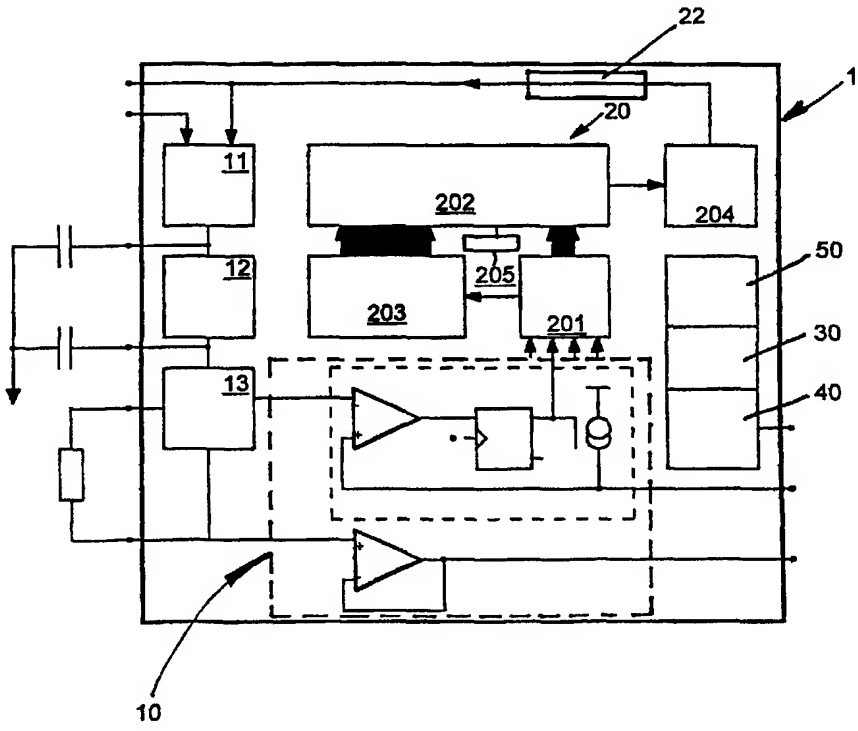
(81) Designated States: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: IMPLANTABLE SENSOR

(57) Abstract

A fully implantable *in vivo* sensor (1) comprises an RF inductive coil transceiver (22, 24), for receiving electromagnetic radiation from a remote control unit to power the sensor and for transmitting data from the sensor. The sensor includes an integrated circuit electrochemical potentiostat (10) and a signal processor from which monitored data is generated and passed to the transceiver for transmission.



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IMPLANTABLE SENSOR

The present invention relates to *in vivo* sensors and, particularly, to implantable sensors which can be used to provide data on biological parameters in the human or animal body by radio telemetry.

Ten years ago a multinational survey of senior clinicians in Europe, North America and Japan identified a range of medical conditions which would benefit from the use of *in vivo* sensors. These included diabetes mellitus, renal/dialysis monitoring, and vital function monitoring in intensive care, anaesthesia and prolonged surgery. Oxygen electrode monitoring systems have been in clinical use for over 35 years for the determination of blood-O_2 levels and the measurement of other blood gases has also become commonplace. In addition, sensors have been proposed to provide for continuous monitoring of blood glucose, see *Trends in Biotechnology 11* 1993, pp285-291, Pickup JC and *Biosensors:Fundamentals and Applications* 1987, Oxford University Press, pp356-375 & 723-736 *Turner APF, Karube I & Wilson GS (Eds.)*. The various prior art sensors reported to date, however, require direct connection either so that data can be readily downloaded from the sensor to a processor and/or because of the need to provide electrical power to the sensor from a battery. Furthermore, such sensors are relatively large in area and therefore problematic for subcutaneous insertion and or implantation.

Although *Enzymatic glucose sensors: Improved long-term performance in vitro and in vivo.* 1994 ASIO Journal 40, pp157-163, Updike SJ, Shults MC, Rhodes KR, Gilligan BJ, Luebow JO & von Heimburg D indicates that the authors have studied the long term behaviour of a battery-powered implanted blood glucose sensor in laboratory animals, implantable blood glucose sensors are not yet available commercially.

There appears to be a growing requirement for a fully implantable blood glucose sensor in order to overcome the various problems highlighted above with existing sensors, and the present invention aims to provide such a sensor.

According to the present invention therefore, there is provided a fully implantable *in vivo* sensor comprising an RF inductive coil transceiver, for

receiving electromagnetic radiation from a remote control unit to power the sensor and for transmitting data from the sensor, an integrated circuit electrochemical potentiostat and a signal processor, for data acquisition, formatting and transmission from the transceiver.

Preferably, a reference voltage generator is integrated in the same integrated circuit as the potentiostat and signal processor. Furthermore, preferably, the integrated circuit also includes a master clock signal generator (or oscillator) and appropriate control logic circuitry.

Preferably, the sensor includes a monolithic (integrated circuit) high voltage diode bridge and linear voltage regulator. This allows the sensor to operate as an inductively powered, or AC or DC powered, transponder with only two external capacitors required off chip.

Preferably, the sensor includes a monolithic (integrated circuit) charge-balancing sigma-delta analogue to digital converter for digitisation of sub-microampere currents.

The sensor may be designed with four independent electrode inputs to allow up to four biological or chemical analytes to be determined simultaneously by one sensor. Alternatively, multiple redundancy measurements can be made on one analyte, or true differential mode measurements on up to two analytes.

The sensor preferably includes a monolithic electrochemical electrode clamp voltage, programmable between 0 and + 600 m V DC via a single off chip resistor.

A fully synchronous digital serial-data output stream at 640 baud may be provided which is pulse width modulated with an embedded clock signal for ease of use in inductive telemetry to facilitate clock extraction and synchronisation at the receiver. The output stream may include even-parity bit and stop and start frames.

Preferably, monolithic (integrated) on-chip reset, master oscillator and logic controller circuitry is provided.

Planar electrochemical electrodes, IC bond pads, and inductive coil may all be metallised onto a (monolithic) double-sided, plated through-hole (PTH),

ceramic substrate to make a highly miniaturised hybrid sensor, suitable for implantation.

Thus there can be provided a minimally invasive sensor which once implanted may be interrogated with a hand-held radio frequency paging device, providing completely pain free, real time physiological monitoring.

It may be possible to use such a device as an overnight hypoglycaemic alarm with a radio controlled beside reader, which allows the patient to sleep whilst being remotely monitored. Conventional finger-prick tests require user to be awake - a major disadvantage. Other needle-type overnight sensors are uncomfortable, and require a cannula or wires from the body to the bedside unit.

A sensor according to the invention does not suffer the disadvantages of other invasive needle or sampling type devices, which because of the cannula can interfere with bathing, swimming and other physical activities.

One example of a sensor according to the present invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a custom-fabricated integrated circuit sensor;

Figures 2 to 14, 16 & 17 are circuit diagrams of various component parts of the sensor;

Figure 15 is a representation of a data output waveform transmitted by the sensor;

Figure 18 is a timing diagram of a state machine implemented in a logic controller for controlling the operation of the sensor; and

Figure 19 shows a photomask pattern used in the manufacture of the example.

The exemplary sensor 1 has a potentiostat 10 which is implemented in a 2 µm BiCMOS technology, which is a mixed IC (integrated circuit) technology combining bipolar and field effect transistors. The combination of bipolar (BJT) with field effect (FET) devices into monolithic devices allows for both the high switching speed and current carrying ability of BJT devices with the very high impedance and low power consumption of FET devices.

The exemplary sensor 1 comprises a four channel electrochemical potentiostat 10, designed and fabricated as a full custom integrated circuit. The device has on-chip power conditioning circuits, including a diode bridge 11 for AC or DC operation, a linear circuit voltage regulator 12 for stability of the supply and a silicon band gap circuit 13 providing a reference voltage. A sophisticated digital control circuit 20 organises data collection, conversion and encoding of electrochemical signals from four external electrodes 21. The electrodes are potential controlled with a current mode feedback loop. A serial data interface 22 is included to allow operation of the device in transcutaneous telemetry applications with the minimum number of off-chip components (figure 1).

Power to the sensor 1 is provided through a high frequency inductive link in the form a pair of coils 24, one in an external control unit (not shown) and one on the ceramic substrate 2 of the sensor. Power detection, rectification and regulation circuits are integrated in the IC1 with the low voltage analog and digital circuits.

Coupling of the radio frequency energy into the implanted sensor is optimised via a resonant tuned LC tank circuit. The inductive and capacitive elements of the tank are not integrated into the IC1, but are hybrid components external to the integrated circuit 2. The integrated diode bridge 11 full wave rectifies the resonant tank voltage, and this supplies the on-chip linear regulator 12 to produce the five volt supply needed for both the analog and digital signal processing circuits.

The RF interface is shown schematically in figure 2. Diodes I$5 - I$8 are arranged in a bridge configuration 11 and convert the RF voltage from the coil at inputs VRF_POS and VRF_NEG to a full wave rectified waveform. With the addition of a hybrid capacitor (not shown) across the outputs Vddu and Vss of the diode bridge 11, an unregulated DC voltage is generated at pin Vddu, with a magnitude approximately equal to the root mean square of the RF amplitude. The ripple voltage at pin Vddu is inversely proportional to the external capacitance, and directly proportional to the load current drawn from the diode bridge 11. A capacitor mounted on the ceramic substrate 2 for decoupling the

power supply was chosen to meet the conflicting requirements of achieving large capacitance, high working voltage rating, but small physical size. By way of example, a 10,000 pF integrated capacitor in the 2 µm HBIMOS process, with a maximum working potential of 40 volts occupies 35 mm^2 of silicon area (approx 6 mm x 6 mm square), compared to 1.0 mm x 0.5 mm x 0.5 mm required for the surface mount capacitor of equivalent value.

Diodes I$5 - I$8 are configured as npn transistors with the base-emitter junction shorted to take advantage of the high breakdown voltage of the collector-emitter junction. The junction has a reverse breakdown potential of 80 volts, compared to 10 volts for the base-emitter junction. The basic transistor cell is further modified with the addition of an NPLUG guard ring to minimise parasitic currents in the silicon substrate. The diodes are rated at 5 mA forward conduction current. The remaining integrated diodes, I$9, I$10 and I$430 provide reverse voltage protection to an NDMOS power transistor, I$2255 which switches the induction loop during reverse telemetry signalling (see later).

The unregulated voltage at pin Vddu is controlled through the linear circuit regulator 12 to +5 volts with respect to the substrate potential, V_{ss}. The regulator 12 is an integrated device designed for maximum energy efficiency, low dropout potential and rapid response. These criteria ultimately determine the ability of the integrated potentiostat to operate continuously and normally during extreme variations in input voltage, such as will occur when the sensor is operated at, or near to, the periphery of the high frequency induction. The linear regulator is shown schematically in figure 3.

The regulator 12 has a closed loop configuration, with an overall voltage gain of 2.1. A sample of the output voltage V_{DD} is taken, at pin V_{DD}, across two high ohmic poly silicon (HIPO) integrated resistors I$6, I$4 and applied to the non-inverting input of the high slew rate comparator, I$1902. The inverting input of this comparator is held at +2.4 volts with respect to pin V_{SS} by the band-gap reference cell, I$1645. The output stage of the comparator cell is optimised for switching and switches NDMOS power transistor I$3524 hard on and off such that the output voltage V_{DD} is maintained at +5 volts (2.1 x the bandgap potential of 2.4 v). A current reference cell is used to bias the comparator I$1902, and

a pull-up resistor I$3726 balances the current in the output transistors with the bias current.

The output terminal V_{DD} of the linear regulator 12 is connected to the V_{dd} power ring of the integrated circuit. and hence supplies power to all remaining circuits on the IC. The band-gap reference cell, current reference cell and comparator cell are operated with their positive supply rails connected to the unregulated DC supply, V_{DDU}

The +2.4 volt band-gap reference cell (I$1645) also feeds a potential divider circuit (see figure 4) formed from two high ohmic polysilicon (HIPO) integrated resistors. The divider circuit produces a potential of +1.8 volts above V_{ss}. The difference between the band-gap reference and the potential divider voltage determines the working potential applied to the electrochemical cells, i.e. in this case 2.4 - 1.8 volts, equal to +600 mV. The band-gap reference potential is available from the output pin of the integrated circuit, VREF1 Likewise, the divider potential appears at pin $R_{ext}1$. This makes it possible to connect external resistors (REXT) between VREF and REXT to vary the cell potential between zero and +600 mV which may be particularly useful in circuit testing and which also allows the same circuit to be used as a sensor for different electro-active species. For potentials greater than + 600 mV an external resistor may be connected between pin REXT and the substrate, V_{ss}.

The counter-reference output terminal of the integrated potentiostat is pin cnt_ref (see figure 5). This output is a buffered version of the potential programmed at pin REXT. The buffer amplifier has MOS inputs and a bipolar output stage configured for unity gain. The output stage of this amplifier can source or sink 300 μA, whilst the amplifier itself requires only 20 μA supply current. With the VREF and REXT pins open circuit, the CNT_REF terminal of the potentiostat is driven at +1.8 volts with respect to V_{ss}.

The sensor will operate with up to four independent working electrodes and a common counter-reference electrode. Each working electrode potential is maintained at +2.4 volts by current-mode feedback (see figure 1). Each working electrode output pin, WRK_01, WRK_02, WRK_03 and WRK_04 is controlled through a switched pnp current mirror cell (see Figure 6).

The current mirrors are programmed to source 1 μA into the working electrode circuit when enabled. The mirrors are programmed with a custom cell comprising PMOS and NMOS transistors organised in a cascode arrangement to form a minimum area active resistor (figure 7). The PMOS and NMOS devices have the required geometry to sink 1 μA when the cascode is switched on through the minimum area NMOS device (W=5 μm, L=5 μm I$3).

At the core of the integrated potentiostat is the analog-to-digital converter (ADC) circuit which measures the current in the electrochemical cells and produces encoded digital words to represent these currents. Of the many conversion techniques available to produce digital representations of analog signals, the over-sampling method is most suitable in the design of the present implantable sensor because the over-sampling converter can have, theoretically, an unlimited number of bits, and hence infinite resolution, it is inherently monotonic and there are no missing codes in the digital output. In its physical manifestation, the over-sampler occupies relatively little silicon area, as it consists almost entirely of digital circuit elements, and it can therefore be made energy, as well as area, efficient in mixed mode silicon process technologies, especially BiCMOS.

The over-sampling, or sigma-delta converter, digitises analogue signals with 1-bit resolution, but at very high sampling rates. The resolution can be increased with digital filtering. It is therefore the ideal architecture for high resolution, low distortion conversion of low frequency signals. A first order over-sampling converter consists of a sigma-delta modulator which converts the analogue input signal into a continuous stream of 1's and 0's at a rate determined by the sampling clock frequency, Kf_s (Figure 8). A digital filter interprets the bit stream at a much lower frequency, f_s, into an n-bit digital word. The ratio of the sampling frequency to the data rate is the over-sampling ratio, K.

In a conventional sigma-delta converter the 1-bit digital-to-analogue converter (DAC) is driven from the serial bit stream, and the averaged output from the DAC will tend to equal the input voltage signal if the loop has sufficient gain (Figure 8). If the number of 1's in the output data stream are counted over

sufficiently large a number of samples. the count value will be a digital representation of the input signal. It is necessary to count for 2^n clock cycles to achieve n-bit resolution.

An adaptation of the basic sigma-delta modulator has been designed for the integrated potentiostat utilised in the present sensor. Because the potentiostat is required to clamp the electrodes of the electrochemical cell at a fixed voltage and to also measure the electrochemical current, a charge balancing technique is employed using a current servo loop to maintain the clamp voltage whilst simultaneously producing an over-sampler stream for data conversion.

Fast comparator cells produce the over-sampler streams for each working electrode (figure 5). The non-inverting inputs of the comparators are connected to the band-gap reference of +2.4 volts, whilst the inverting inputs monitor the potentials at the working electrodes of the cell. Any deviation in electrode potential from the reference value causes the output states of the comparators to change; high when the reference potential is greater; low when the electrode potential is greater. The asynchronous bit stream from the comparators is digitally sampled with D-type flip-flops I$2 - I$5 (figure 9) at the over-sampling frequency of around 20 kHz. Sampling the data converts it from an asynchronous stream to a synchronous data series. The sampled data stream is fed back to the pnp mirrors which source current into the working electrodes to keep them at a potential of +2.4 volts. The charge balancing servo loop is therefore closed, and any deviation in working electrode potential from +2.4 volts is immediately compensated for.

A 9-bit binary ripple counter 203 (figure 1) which covers the digital codes 000_{10} to 511_{10} integrates the sampled-data stream (figure 10). Initially the counter is reset to the all zero condition. At the start of an integration period, the counter is enabled and clocked at the over-sampling frequency. The counter value increases when the sampled-data stream is 'high' and holds its count value when it is 'low'. At the end of the integration period, the counter is disabled and the final value will be proportional to the time-integral of the sampled-data stream over the integration period, which, by virtue of the charge-

balancing circuits, is proportional to the current in the electrochemical cell. The integration period is nominally 25 ms, hence digital words are produced at a rate of 40 per second. The over-sampling ratio, K, in this case, is equal to 500.

Each of the four working electrodes has a dedicated charge balancing modulator comprising the comparators, D-type flip-flops and current mirrors (figures 5,6 & 9). However, to minimise silicon area, one digital counter serves to integrate the data from all four channels. The data from each of the four individual sigma-delta modulators is time division multiplexed and sent sequentially to the counter through a four channel digital multiplexor 201 (figures 1 & 11).

The latched count value at the end of the integration period is a parallel 9-bit digital word proportional to the electrochemical cell current. Prefixed to this 9-bit word is the 2-bit binary address of the working electrode from which the data has come. Additionally, a 1-bit even parity code is appended to make an overall word-length of 12-bits. The full 12-bit word is held in a parallel-in-serial-out shift register 202, and is clocked serially out of the register during the next sample integration period. The shift register is made from D-type flip-flops (figure 12). These are D-type cells with individual set and reset inputs. The address, data and parity bits are latched when the parallel-load control line is asserted high. The shift register cell has two other control inputs, namely a positive edge triggered clock input and a clock enable input which is active when asserted high.

The even parity-bit is generated for the 9-bit data word and 2-bit electrode address. The parity generator 205 is a combinational exclusive-OR logic circuit, implemented from 12 2-input EXOR gates (figure 13). The parity bit is appended to the address and data bits to complete the 12-bit word.

The 12-bit word containing address, data and parity information is synchronously clocked out of the potentiostat using a serial pulse width modulation technique after addition of start and stop codes . The nominal baud rate of the output stream is 640 bits per second; this allows the three start bits, the 12-bit word, and two stop bits to be transmitted in under 27 ms. The pulse

modulator (figure 14) consists of a synchronous 1 of 4 ring counter 204. clocked at one eighth of the master oscillator frequency.

The pulse width coding scheme generates a synchronising pulse stream which is always present at a frequency equal to 1/4 (nominally 640 Hz) of the ring counter clock. The synchronising pulse is the first output bit of the 1 of 4 ring counter. The presence of the synchronising pulse allows receiving equipment to lock onto the transmission stream and to regenerate the clock signal. It has a mark to space ratio of 1:4. Start, stop and data information are then encoded into the synchronising stream by varying the mark to space ratio (pulse width) from 1:4 up to a maximum of 3:4 in discrete steps; 1:4, 2:4 and 3:4. Start and stop frames are uniquely identified by utilising the maximum mark to space ratio of 3:4. Data bits only use pulse widths of 1:4 (data bit = 0) and 2:4 (data bit = 1) and are discriminated at the receiver on that basis. Fig. 15 shows a typical transmission sequence.

The pulse width modulated data stream is applied to the gate of NDMOS transistor, I$2255, through a digital buffer cell 22 (figures 1 & 2). When the transistor conducts, it shorts the resonant tuned LC tank circuit terminals connected at pins VRF_POS and VRF_NEG. Integrated diode I$9 protects the transistor from reverse conduction during the negative half of the ac input cycle. Diode I$10 clamps the source terminal of the transistor at V_{ss} during positive half cycles, and diode I$430 both protects the transistor against reverse drain-source voltage and clamps the source to V_{ss} during negative half cycles. The changes produced in the impedance of the LC tank as a result of the NDMOS switching are reflected in the primary coil of the induction loop as changes in current.

A master oscillator 30 (figure 1) shown in more detail in figure 16, is provided by a MOS inverter gate, I$1, configured with an integrated RC feedback network across its input and output terminals and produces a master clock waveform at a nominal 20 kHz. Resistor I$2 is a high ohmic poly silicon layer resistor of value 1 MΩ, and I$3 an NPLUG capacitor of 22 pF. The clock waveform is buffered through several further inverters, I$9 and I$10, and is used as the clock for the over-sampling converter and charge balancing circuits.

A 3-stage ripple counter, driven from the master clock, generates the eighth sub-harmonic at a nominal 2560 Hz, and this is used to clock the pulse width modulator circuit. The OSC_IN terminal was for software simulation of the clock circuit only, and was never implemented in hardware.

On application of power to the integrated potentiostat a reset signal is generated to force the logic circuits into a known condition. The power-on reset circuit 40 (Fig. 1) detail (figure 17) comprises an integrated RC circuit with a time constant of 100ms. The capacitor I$2 charges through resistor I$1 from V_{dd} and the output of inverter I$3 toggles from high to low approximately 25 ms after power-on. Buffer I$411 inverts the reset signal to active-low. The minimum required pulse duration to guarantee reset of the logic gates is specified as 25 ns when V_{dd} = 15 volts. An external connection to the reset circuit is available via pin RESET of the IC, which may normally be left open circuit (figure 1). Shorting this pin to V_{ss} will reset the device. In the reset condition the 9-bit counter is cleared, the multiplexor address is set to zero, and both the pulse width modulator ring counter and the state machine timers (50, fig. 1) are cleared.

Overall control of the integrated potentiostat is maintained by a sequential circuit state machine or logic controller 50 (figure 1). The timing diagram for the state machine 50 is shown in figure 18. All timing intervals and logic conditions generated by the state machine are derived from the master oscillator and are synchronous with it. Therefore the periods of the control pulses are nominal only, and based on a master oscillator frequency of 20kHz. The advantage of employing a synchronous system is that timing relationships between all control and data signals are fixed, irrespective of variation in the master clock rate, and therefore the occurrence of race conditions or incomplete data sampling is completely avoided.

After reset, a sampling period is enabled for the first working electrode (/cnt_enbl); this enables the 9-bit counter and it begins to integrate the data stream. At the end of the sample period, the counter is stopped and the value latched into the shift register along with the electrode address and the parity bit (/pl_load). Finally the counter is cleared to zero again, the multiplexor address

incremented by one, and the sequence begins for the second electrode (/reset). After all four electrodes have been sampled in this way, the cycle begins again with the first electrode.

Whilst the potentiostat is busy sampling the current in one of the four electrochemical cells, it simultaneously transmits the previously acquired sample via the passive telemetry loop. At the initiation of a new sampling period, the start of transmission frame is also enabled (/frame_enbl). When three sequential start bits have been transmitted, the start frame is disabled and the data frame is enabled (/data_enbl). This allows transmission of the previously stored twelve-bit word. Finally, the data frame is disabled and the stop frame enabled for the last two successive bits (/frame_enbl). Due to the synchronous nature of the system, these seventeen bits of information take precisely one complete sample cycle to transmit. In this way, it is impossible for the sensor to acquire data faster than it can transmit it, resulting in a continuous flow of information which is inherently free from overrun errors.

In the successful development of an integrated potentiostat within an implantable sensor the problem of lack of compatibility between semiconductor processing techniques and the materials necessary to implement a micro-electrochemical cell with a sensing layer have to be addressed. The solution adopted for the example is a *hybrid* device.

Miniaturised electrochemical electrodes can be fabricated by thick or thin film deposition and photolithographic processing methods, and whilst these processes are directly compatible with the electronic circuit fabrication techniques, the materials needed are entirely different. Electrodes are fabricated from thick or thin films of platinum, deposited by sputter deposition, and reference electrodes can be formed from electroplating with silver and silver-chloride.

An example of this process is for a glucose sensor where the biological sensing layer, the membrane which gives the sensor its specificity, must be immobilised onto the electrode surface. The enzyme layer is sensitive to its environment, especially temperature and pH variations, and is easily denatured by exposure to extreme conditions. This therefore limits handling and storage

options during the processing of the micro-electrochemical cell to make a sensor. In order to separate out these components in the development of an implantable glucose sensor, a hybrid process was therefore adopted. This has allowed for independent fabrication and processing of the parts, and this approach in general, potentially improves the overall manufacturing yield as each component can be proven before it is incorporated into the final sensor.

The construction of the implantable glucose sensor was divided into sequential phases. The potentiostat circuit and associated electronic processing circuits were designed and implemented on a mixed-signal integrated circuit as described above. The decision to keep the electrodes for the sensor off the chip was deliberate and formed part of the overall strategy of designing a hybrid sensor. The decoupling and power supply storage capacitors were also off chip, along with the components used to make the tuned circuit for the RF induction link. The advantages of fabricating a hybrid rather than a monolithic device included having a choice of electrode metals (gold, platinum, silver/silver-chloride etc.), greater electrode area for an improved signal, independent processing of the substrate from the integrated circuit, thereby allowing for aggressive chemical and aqueous processing, simpler device encapsulation, and independent characterisation and testing of the electrodes from the IC.

The off-chip electronic components and the electrodes were incorporated into, or attached, as appropriate, to a ceramic substrate. The alumina (Al_2O_3) substrate is patterned with metallised tracks to make the interconnects between the chip and the off chip components. The electrochemical electrodes and RF coil were also defined at this time by the same metallisation process. Hence the substrate only required some post-fabrication to create the necessary electrode surfaces, attachment of the surface mount capacitors, and then finally, immobilisation of a glucose oxidase membrane as the last step.

A metallised layer was patterned onto one side of an alumina substrate. The alumina substrates had been obtained as wafers measuring 10 cm x 10 cm, and were laser scribed into rectangles with radiused corners measuring 14 mm x 9 mm. This defined the outline size of the hybrid sensor. Whole wafers

were cleaned and then metallised with gold in an evaporator system using well-known techniques. After metallisation, the wafers were cut along the scribe lines into individual substrates and patterned photolithographically, before being etched. The photomask pattern is shown in figure 19, and was produced on a commercial chrome-on-glass mask. In a larger scale production environment, the ceramic wafers could be metallised, patterned and etched all prior to cutting into die, which would significantly improve yield. This would be particularly true if contact photolithography was used.

In accordance with the example described, there are four electrodes 21 on the substrate surface, each measuring approximately 700 µm x 700 µm (0.5 mm^2). The working electrodes are routed by metallisation to the chip, and a fifth, common counter-reference electrode 23 both surrounds them and isolates them from one another. Along the outside edges of the substrate is patterned the RF induction coil 24, which comprises 5 turns of 66 µm wide track (pitch 100 µm). This was tuned with one of the surface-mount capacitors, which were bonded to the substrate with silver loaded epoxy paint. The integrated circuit was attached and wire bonded onto the appropriate pads.

CLAIMS

1. A fully implantable *in vivo* sensor comprising an RF inductive coil transceiver, for receiving electromagnetic radiation from a remote control unit to power the sensor and for transmitting data from the sensor, an integrated circuit electrochemical potentiostat and a signal processor, for data acquisition, formatting and transmission from the transceiver.

2. A sensor according to claim 1, further including a reference voltage generator.

3. A sensor according to claim 2, wherein the reference voltage generator and signal processor are integrated into the same integrated circuit as the potentiostat.

4. A sensor according to any of claims 1 to 3, wherein the integrated circuit also includes a power interface and conditioning circuitry, a sensing electrode interface and conditioning circuitry, and a data-telemetry interface and control circuitry.

5. A sensor according to any of claims 1 to 4, wherein the integrated circuit also includes a master clock signal generator (or oscillator) and appropriate control logic circuitry.

6. A sensor according to any of claims 1 to 3, wherein the integrated circuit also includes a monolithic (integrated circuit) high voltage diode bridge and linear voltage regulator.

7. A sensor according to any of claims 1 to 6, which includes a monolithic (integrated circuit) electrochemical electrode clamp voltage, programmable between 0 and + 600 m V DC via a single off chip resistor.

8. A sensor according to any of claims 1 to 7, which includes a monolithic (integrated circuit) charge-balancing sigma-delta analogue to digital converter for digitisation of sub-microampere currents.

9. A sensor according to any of claims 1 to 8, which includes a fully synchronous digital serial-data output stream at 640 baud which is pulse width modulated with an embedded clock signal for ease of use in inductive telemetry to facilitate clock extraction and synchronisation at the receiver.

10. A sensor according to any of claims 1 to 9, wherein the sensor has four independent electrode inputs to allow up to four biological or chemical analytes to be determined simultaneously by one sensor, to allow multiple redundancy measurements to be made on one analyte, or true differential mode measurements on up to two analytes.

11. A sensor according to any of claims 1 to 8, further including a sensing electrode array.

12. A sensor according to claim 11, the sensor array having planar electrochemical electrodes, IC bond pads, and inductive coil all metallised onto a monolithic substrate.

13. A sensor according to any of claims 1 to 12, adapted for use as a blood glucose sensor.

14. An overnight hypoglycaemic alarm incorporating a sensor according to any of claims 1 to 13, to allow a patient to sleep whilst being remotely monitored.

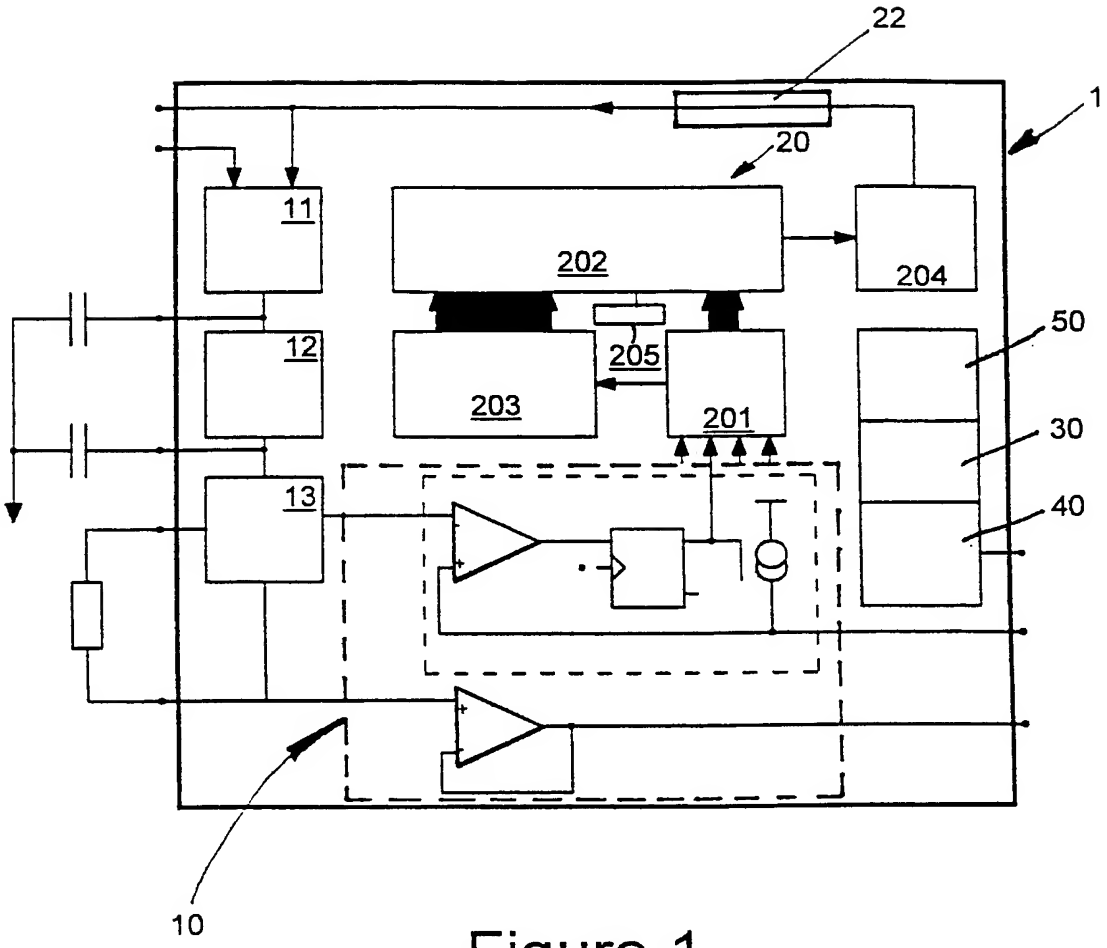


Figure 1

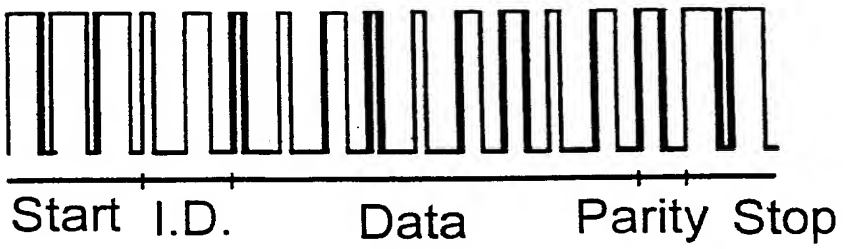
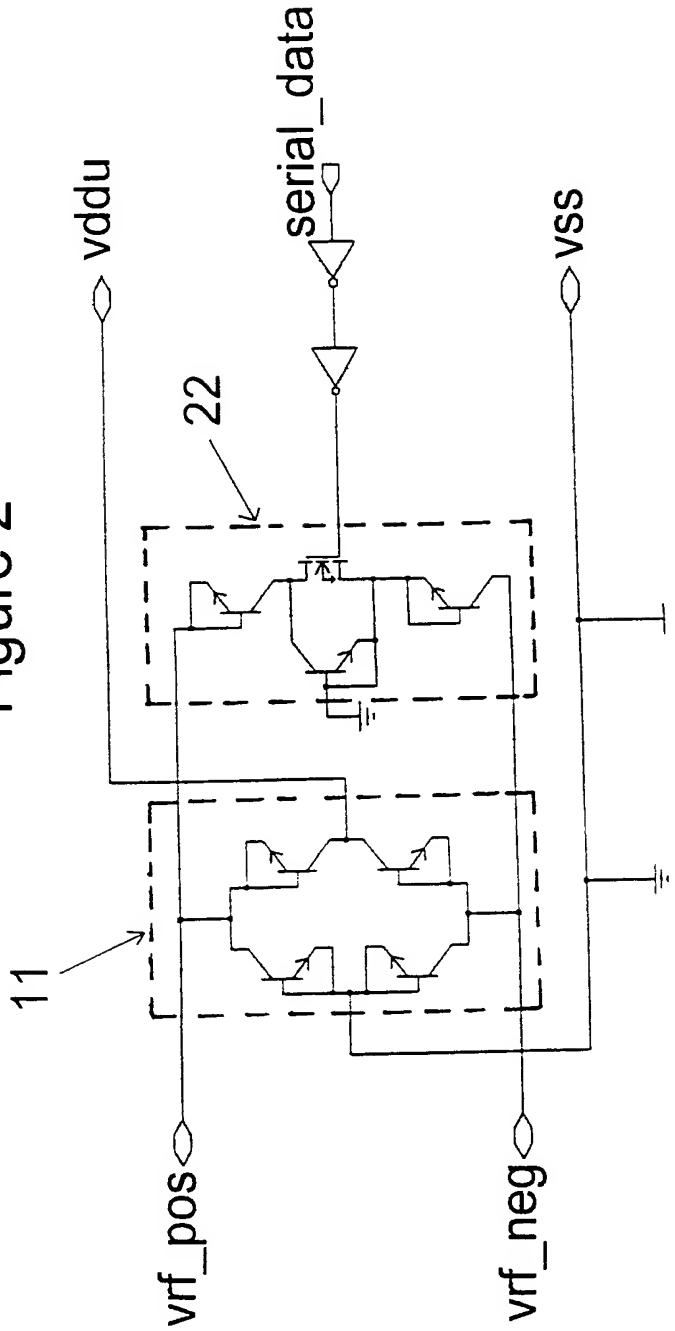


Figure 15

Figure 2



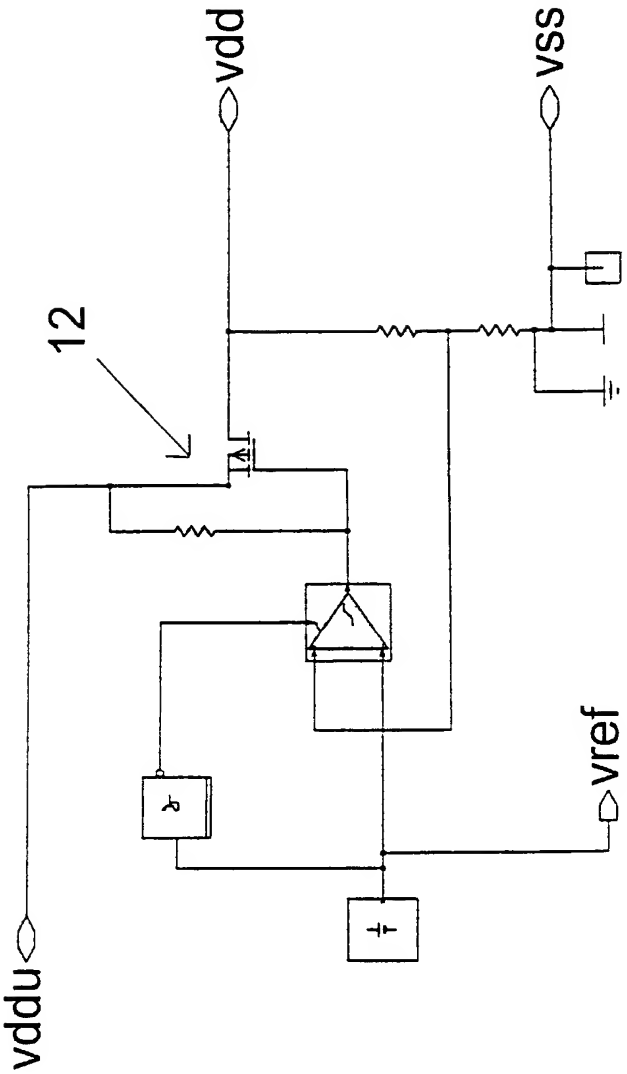
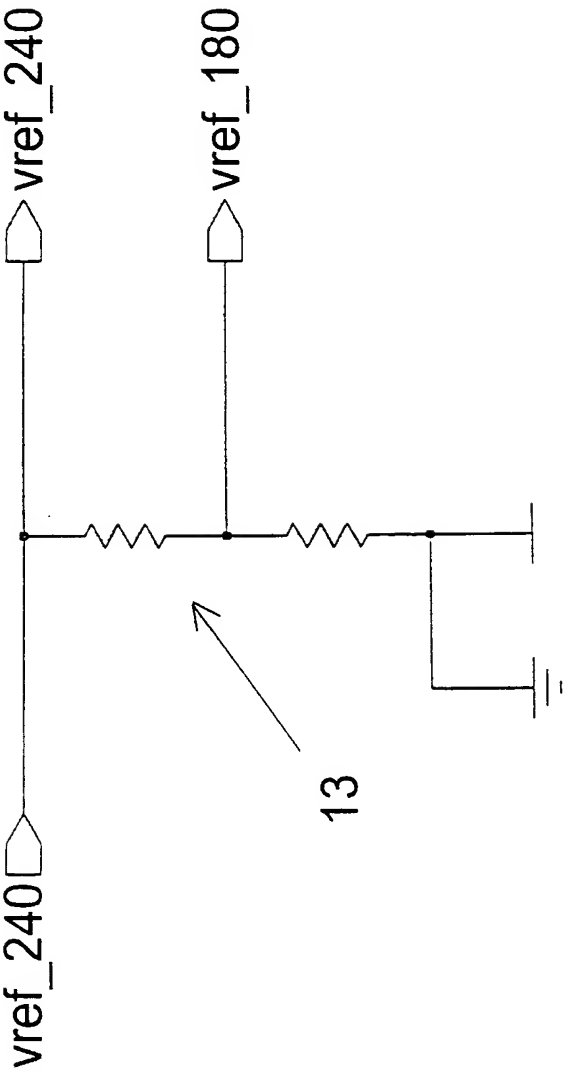
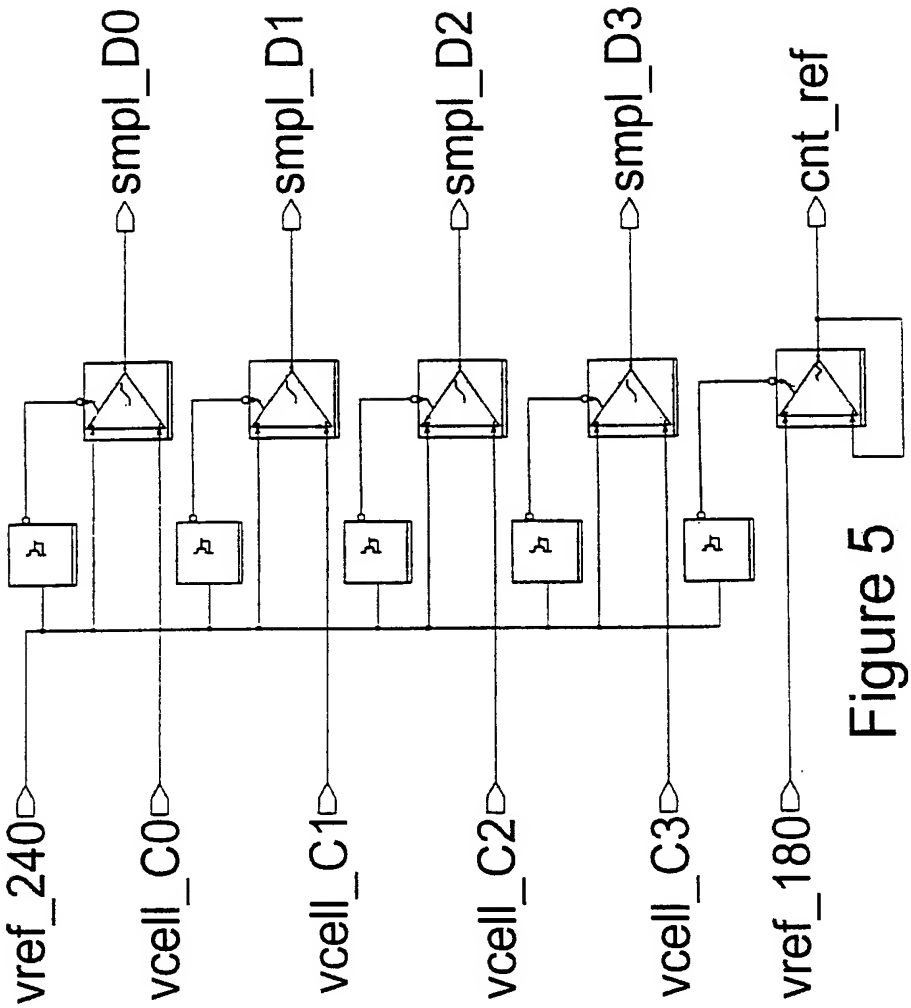


Figure 3

Figure 4

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smpl_D1
smpl_D2
smpl_D3
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vref_240
vcell_C0
vcell_C1
vcell_C2
vcell_C3
vref_180

Figure 5

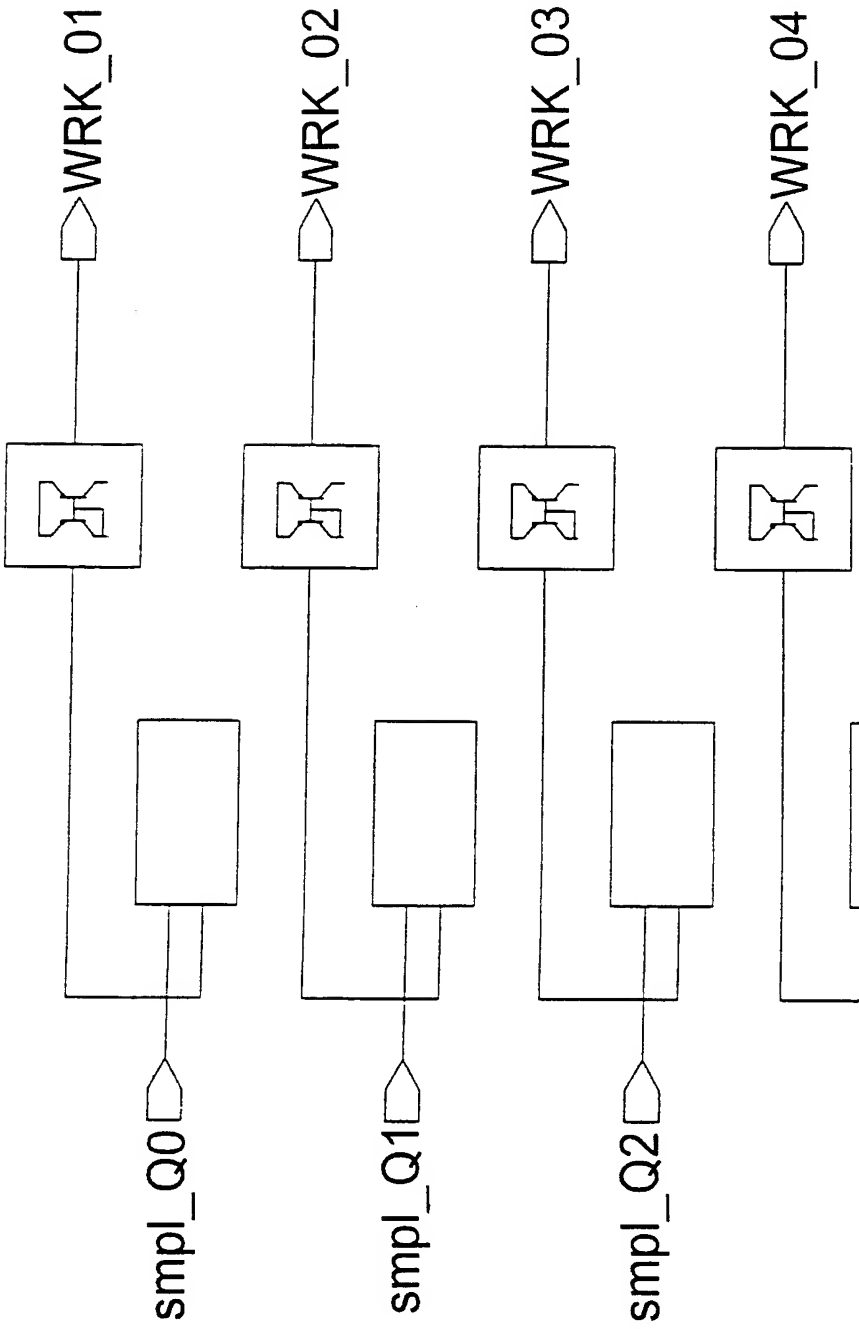


Figure 6

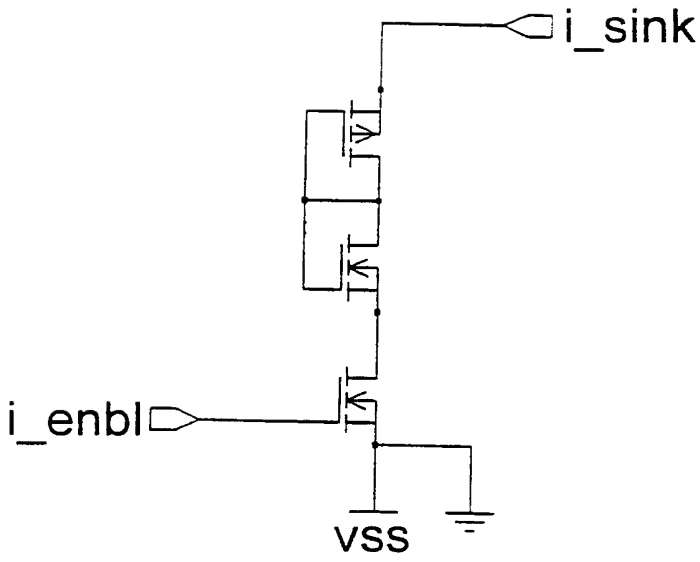
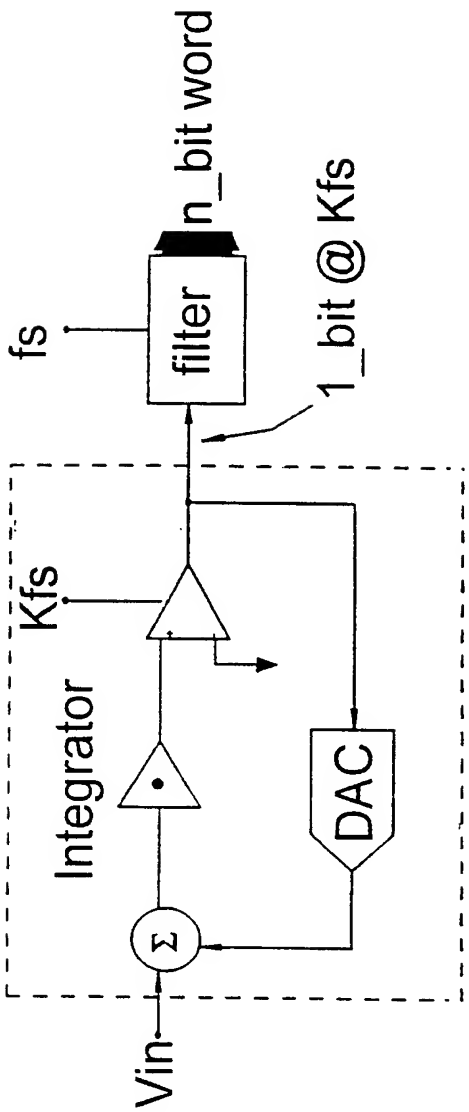


Figure 7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fs
filter
1_bit @ Kfs
Kfs
Integrator
DAC
Σ
Vin
Sigma Delta Modulator

Figure 8

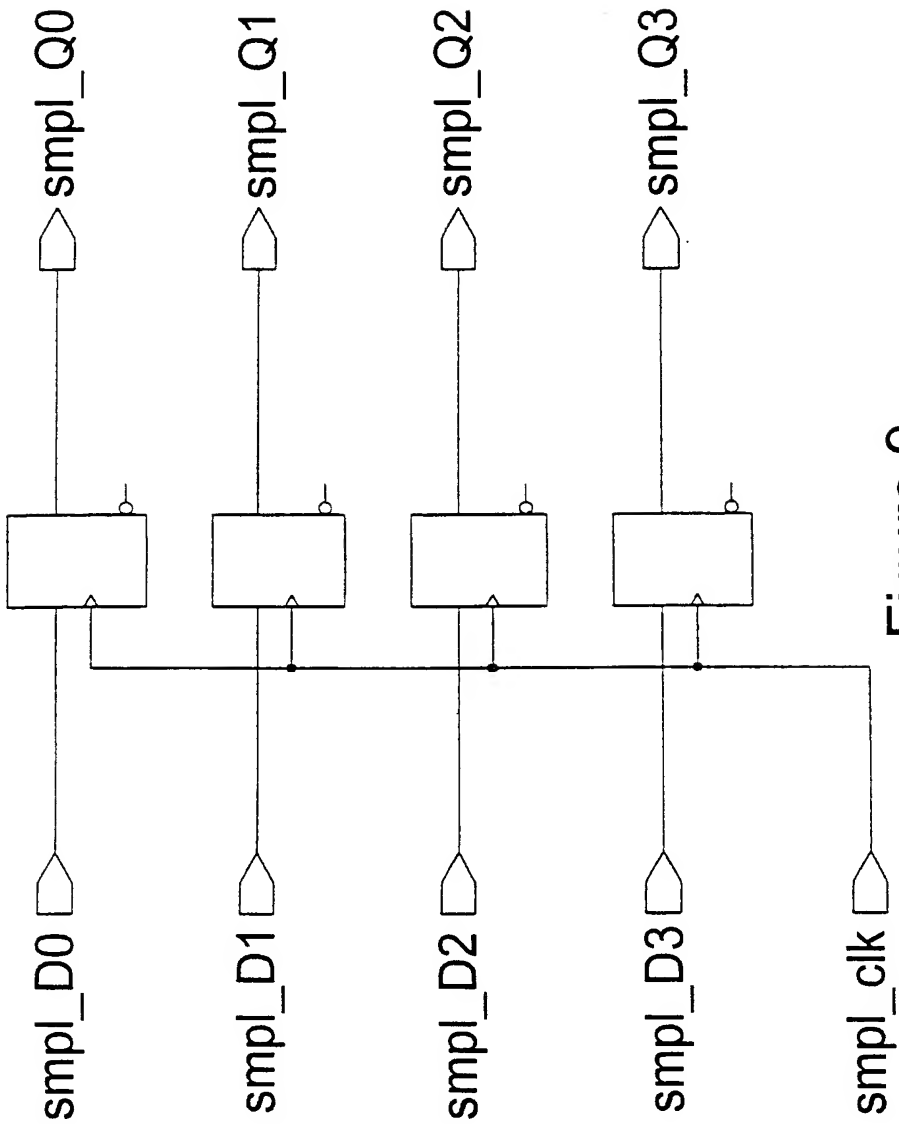

smpl_Q0
smpl_Q1
smpl_Q2
smpl_Q3
smpl_D0
smpl_D1
smpl_D2
smpl_D3
smpl_clk

Figure 9

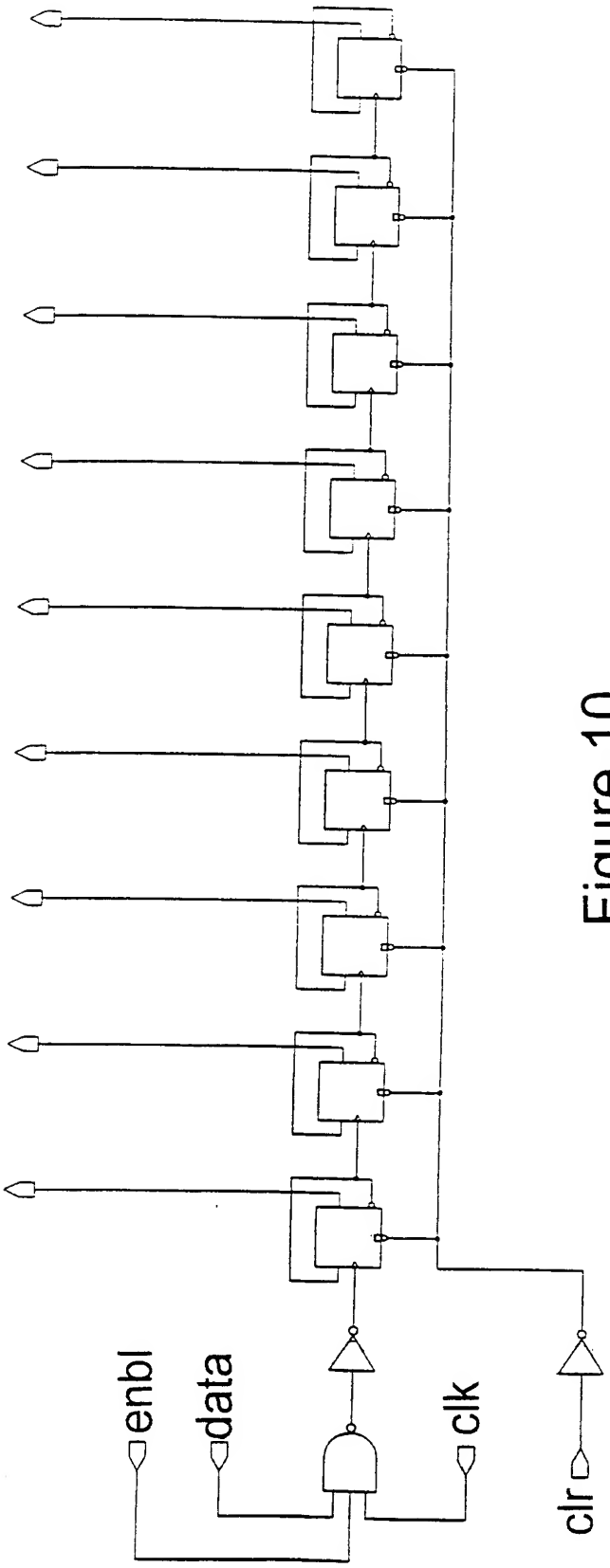
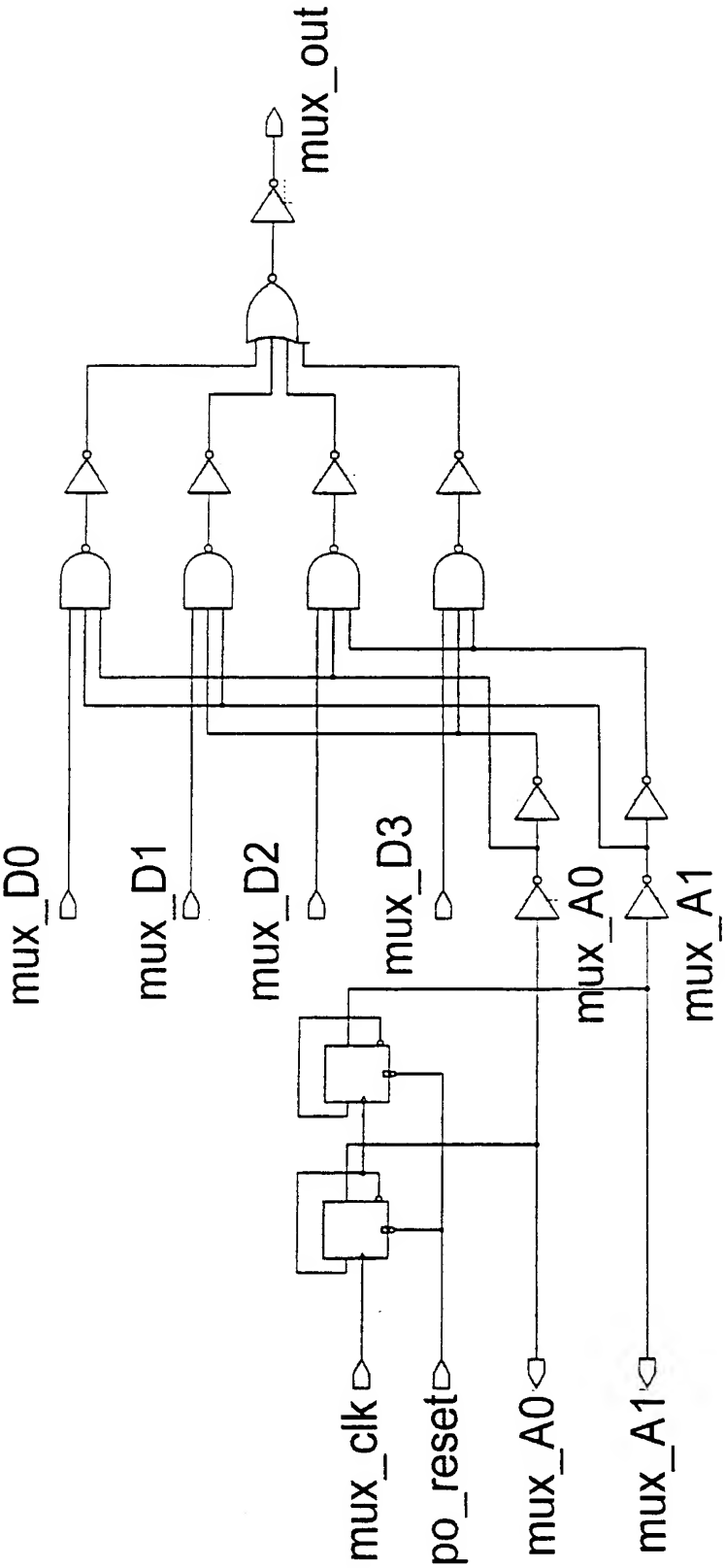


Figure 10


mux_out
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mux_D1
mux_D2
mux_D3
mux_A0
mux_A1
mux_clk
po_reset
mux_A0
mux_A1

Figure 11

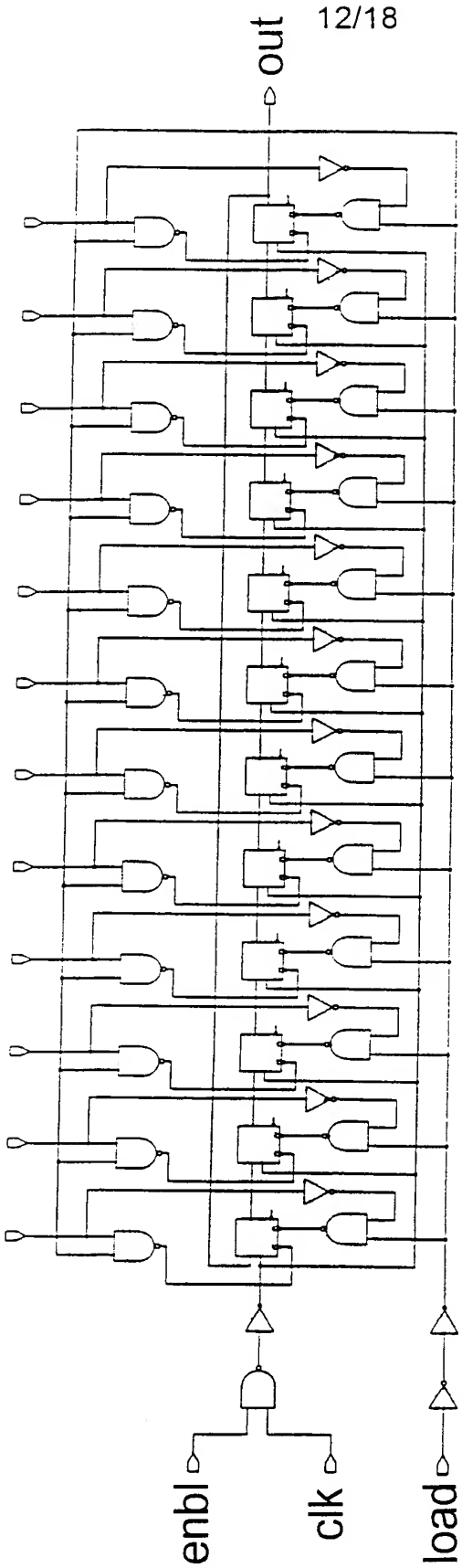

Figure 12

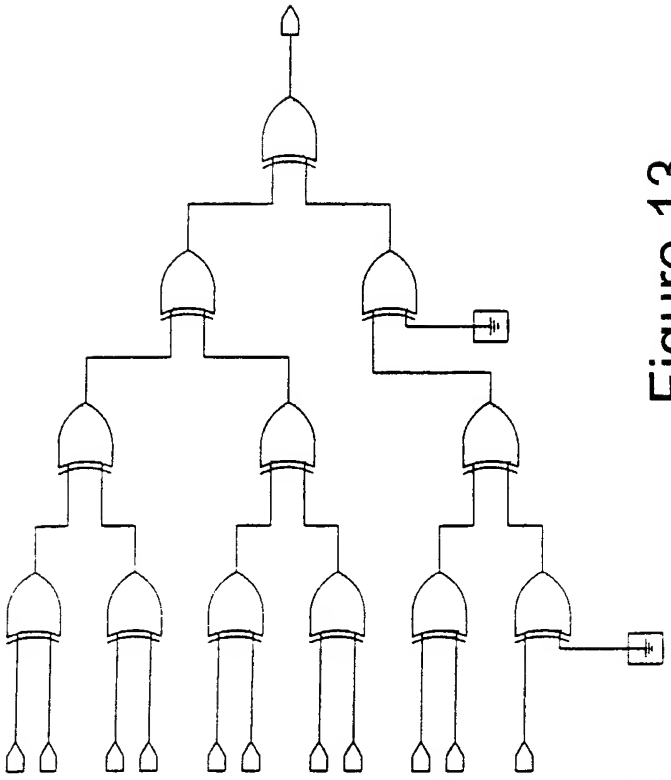

Figure 13

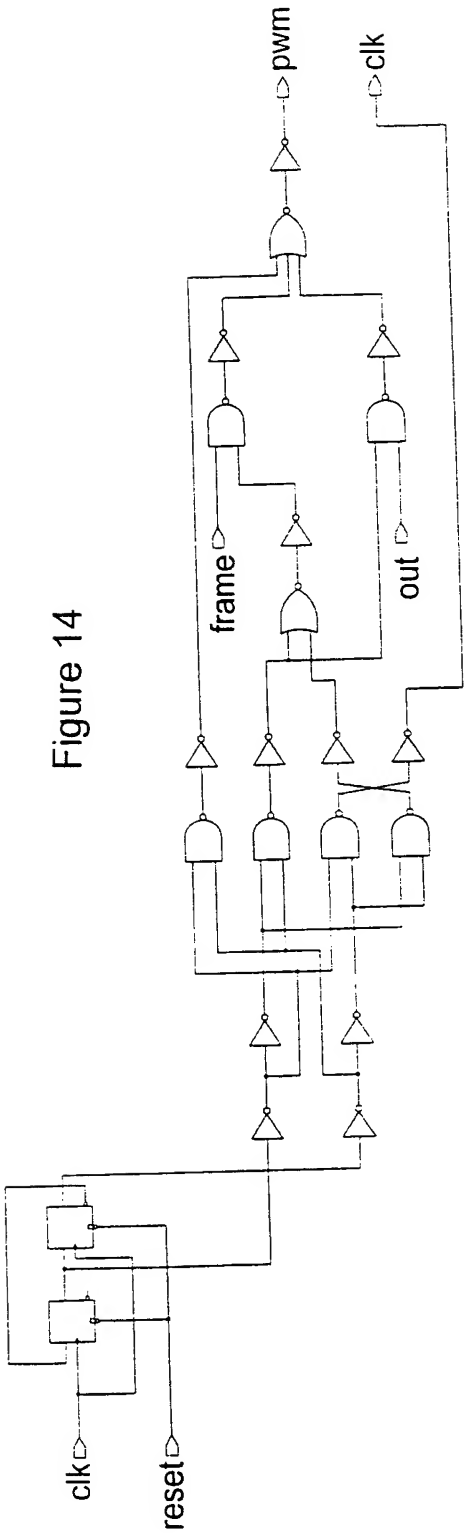

Figure 14

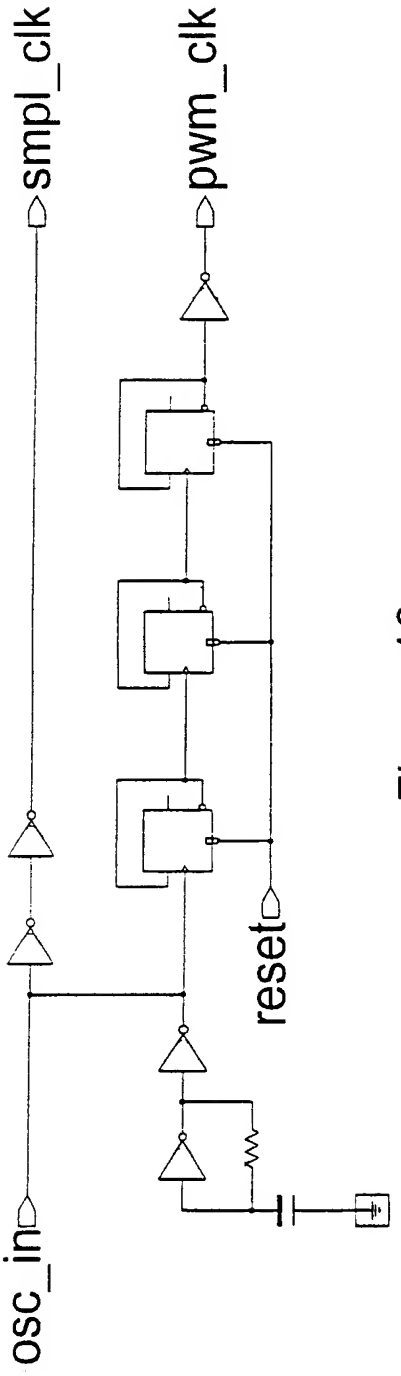

Figure 16

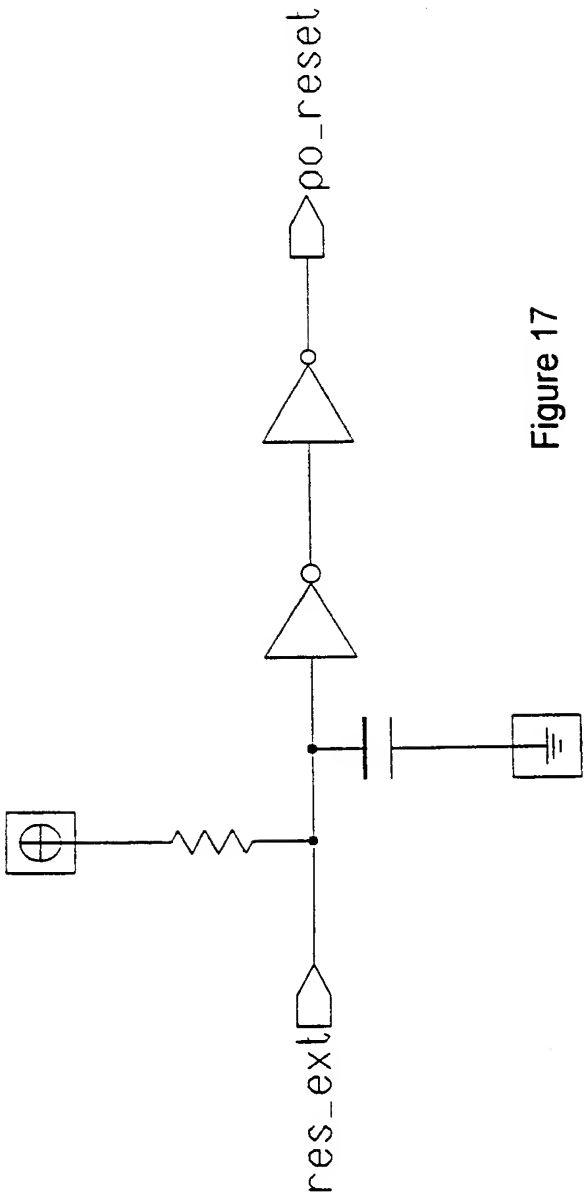

Figure 17

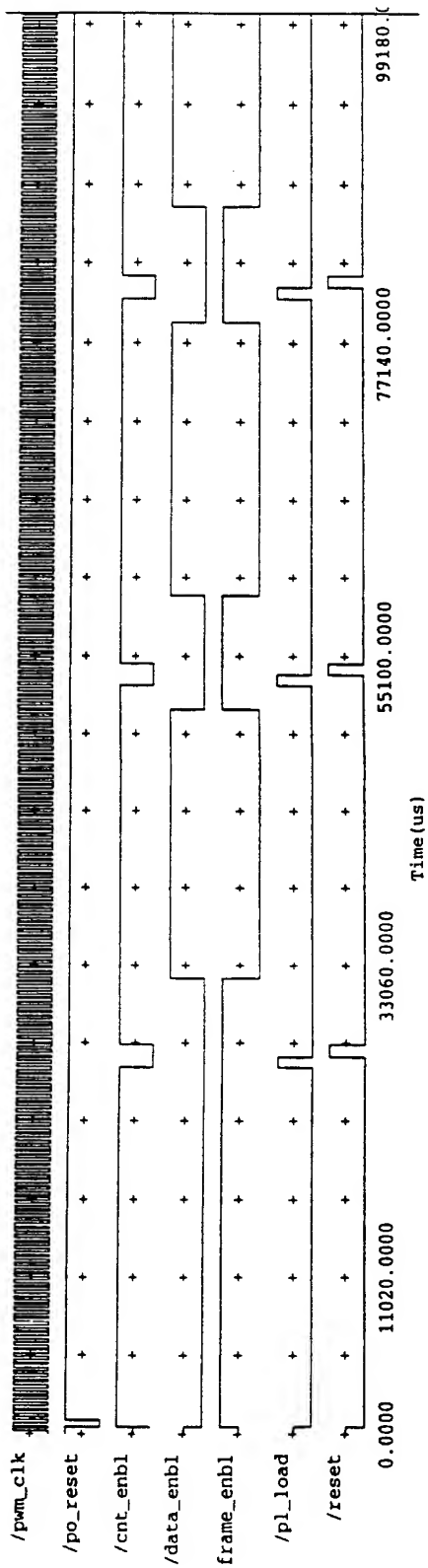
/pwm_clk
/po_reset
/cnt_enbl
/data_enbl
/frame_enbl
/pl_load
/reset
0.0000
11020.0000
33060.0000
55100.0000
77140.0000
99180.
Time(us)

Figure 18

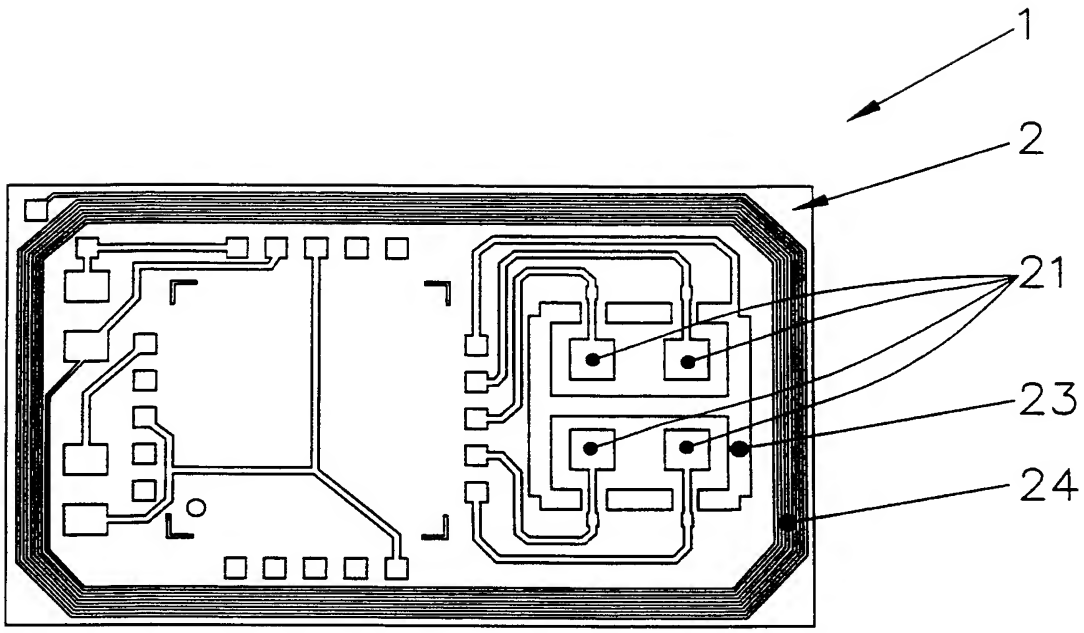

Figure 19

INTERNATIONAL SEARCH REPORT

Interr ıal Application No
PCT/GB 00/01268

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 A61B5/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 A61B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SALEHI C ET AL: "A TELEMETRY-INSTRUMENTATION SYSTEM FOR LONG-TERM IMPLANTABLE GLUCOSE AND OXYGEN SENSORS" ANALYTICAL LETTERS,US,NEW YORK, NY, vol. 29, no. 13, 1996, pages 2289-2308, XP000889776 ISSN: 0003-2719 sections "2. Potentiostats" and "4. Transmitter Subunit" --- -/--	1,2,4,6, 7,10,13

[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 June 2000	12/07/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Knüpling, M

2

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/GB 00/01268

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	REAY R J ET AL: "AN INTEGRATED CMOS POTENTIOSTAT FOR MINIATURIZED ELECTOANALYTICAL INSTRUMENTATION" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE,US,IEEE INC. NEW YORK, vol. 37, 1 February 1994 (1994-02-01), pages 162-163, XP000507101 ISSN: 0193-6530 page 162, right-hand column figure 4 ---	1-3,5,6, 11,12
A	AKIN T ET AL: "A WIRELESS IMPLANTABLE MULTICHANNEL DIGITAL NEURAL RECORDING SYSTEMFOR A MICROMACHINED SIEVE ELECTRODE" IEEE JOURNAL OF SOLID-STATE CIRCUITS,US,IEEE INC. NEW YORK, vol. 33, no. 1, 1 January 1998 (1998-01-01), pages 109-118, XP000766624 ISSN: 0018-9200 section "V. Conclusions" -----	1,2,4-6, 9

2